a gate oxide layer provided on an inner surface of each of said trenches and on the surface of said semiconductor substrate;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate oxide layer and connected to said gate wire, with one set of said trench gate electrodes being constituted by twos arranged in sequence at the first distance (L5), and said first distance (L5) is greater than said second distance (L6);

an N-type emitter layer provided in the surface part of said P-type base layer having a length of said second distance (L6) interposed between said trench gate electrode belonging to said one set of electrodes and said trench gate electrodes belonging to another set of electrodes adjacent to said one set of electrodes, and in the vicinity of said trench gate electrode;

an insulating oxide layer provided covering a part or the whole of said trench gate electrode, and holed with contact holes at each of portions provided with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating oxide layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on said P-type emitter layer on the underside of said semiconductor substrate;

wherein the predetermined depth of the trench is set to such an extent that a depletion layer formed extending from a top of said trench gate electrode when in a forward voltage application is fused with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is

A1 Concl'd.

vicinal and that a curvature of said depletion layer at the top of said trench gate electrode is relieved.

Please add new Claims 11-14 as follows:

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11. (New) An insulating gate type semiconductor device according to Claim 7, wherein the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3 μm or less.

12. (New) An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof;

a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate, said plurality of trenches constituting a set of trenches, each set of trenches being disposed at an interval having a first distance (L5), each of said set of trenches having a second distance (L6) between both end trenches, and said first distance (L5) is greater than said second distance (L6);

an N-type emitter provided in the surface part of said P-type base layer having a width of the second distance;

a gate oxide layer provided at least on an inner surface of each of said trenches;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate oxide layer and connected to said gate wire;

an insulating oxide layer provided covering said trench gate electrode, and holed with contact holes at each of portions with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating oxide layer and connected to said P-type base layer and said N-type emitter layer; and